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REMARKS

I. Status

In the Office Action mailed April 24, 2003, the Examiner noted that claims 1-6 were pending and rejected claims 1-6. The applicant respectfully traverses the rejection.

II. Responsive to Communication

The Examiner indicated the Office Action mailed April 24, 2003 was responsive to a communication filed on October 9, 2002. According to our records, the Office Action mailed 24, 2003 was responsive to the filing of the Application on February 5, 2001. The Applicants respectfully request a correction of the record.

III. Oath Declaration

The applicant respectfully requests that the applicant be permitted to submit a supplemental declaration after allowance which will also include the minor correction noted by the Examiner.

IV. Double Patenting

The applicant respectfully traverses the rejection that claims 1-6 are unpatentable over claims 1-10 of U.S. Patent 6,122,315. Claims 1-10 of U.S. Patent 6,122,315 recite a video decoder comprising a spatial decoder connected to a source of coded video data; a temporal decoder; and a video formatter, receiving data from at least one of said temporal decoder and said spatial decoder, wherein said temporal decoder and said spatial decoder define a data source, a data memory for storing the received data. Claims 1-10 do not disclose, as recited in claims 1-16 of the present invention "a pipeline system

for decoding a data stream" nor the elements of "a sequence of pipeline stages", and a pipeline stage being "reconfigurable". Since the video decoder of claims 1-10 of U.S. Patent 6,122,315 does not recite the elements of a pipeline system of claims 1-6 of the present invention, it would not have been obvious to a person of skill in the art to have recognized the pipeline system of claims 1-6 based on the claims of U.S. Patent 6,122,315. Therefore the claims of the present invention are patentably distinct from the claims of U.S. Patent 6,122,315.

The Applicants submits a Terminal Disclaimer for the purpose of overcoming the double patenting rejection of U.S. Patent 6,263,422. However, Applicants do not admit to any characterization or limitation of the claims by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

V. Foreign Priority

Certified copies of the priority documents EP 92306038.8, GB 9405914.4, and GB 9504046.5 were submitted in the parent application 09/307,239. Hence, applicants request that the Examiner acknowledge receipt of these foreign documents.

VI. Rejection of claims under 35 U.S.C. § 103(a)

Claims 1-2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horvath et al. in view of Ueda et al.

To support the allegation that Horvath et al. discloses at least one of the pipeline stages being reconfigurable to operate according to different standards, the Examiner cites to column 2, lines 45-55 and column 9, lines 13-38 of Horvath et al. Column 2, lines 45-55 of Horvath et al. teaches the storage of the data associated with an image block along with the control information for that image block. Similarly, column 9, lines 13-38 of Horvath et al. teaches a "method for sequentially processing a plurality of data block" (column 9, lines 32-34). However, the above-stated sections of Horvath et al. does not disclose

a "sequence of pipeline stages" (claim 1, line 3) nor does it disclose a pipeline stage which is "reconfigurable to operate according to...different standards" (claim 1, line 4). In fact, Horvath et al. teaches a sequential process (column 9, line 33) for operating on blocks of data in a buffer memory. Furthermore, the disclosure is silent as to the processing of different standards.

To support the allegation that Horvath et al. discloses the at least one of the pipeline stages including processing circuitry with an active state which is entered when the data received by the at least one of the pipeline stages has a predetermined activation pattern corresponding to on of the different standards, the Examiner cites to Figure 1, element 18, column 4, line 61 to column 5, line 30, and column 6, lines 1-16. Figure 1, element 18 shows a local state machine (LSM) which is used to coordinate the processing of image blocks and the decode process (column 5, lines 1-2). Column 4, line 61 to column 5, line 30 discloses how the LSM passes blocks of data to the CODEC 24. Column 6, lines 1-16 discloses the steps of a single standard; i.e the JPEG standard. Consequently, the above-stated sections of Horvath et al. show the interactions between the LSM and CODEC and do not disclose a pipeline stage, or a pipeline stage with an "active state" entered when the data has a "predetermined activation pattern" (claim 1, line 7). Furthermore, Horvath et al. is silent as to processing of "different standards" (claim 1, line 8) and the cited section column 1-16 does not disclose "different standards" but disclosing the steps of a single standard, namely the JPEG standard.

To support the allegation that at least one of the pipeline stages includes a state machine having a current state and a previous state, the Examiner cites to sections column 1, lines 59-61 and column 5, lines 15-30. Column 1, lines 59-61 discloses decoding of blocks of image data. Column 5, lines 15-30 discloses how the LSM reading data from the Input FIFO 28 and how the data is transferred to the CODEC. Thus, the above-mentioned sections of Horvath et al. merely disclose the coordinating steps between the LSM and CODEC in processing image blocks, and do not disclose a "pipeline stage" including a "state machine".

The Examiner concedes that Horvath et al. does not disclose, inter alia, a sequence of pipeline stages. The Examiner provides the reference Ueda et al., particularly Figure 4, for its disclosure of a sequence of pipeline stages. However Ueda et al. discloses a pipeline architecture having fetch, decode and execute stages, used to process machine instructions. Ueda et al. is silent as to processing image processing blocks, and in fact would not work in processing image blocks since it is a different architecture designed to process machine instructions.

Furthermore, Ueda et al. processes machine instructions using an instruction fetch (IF) stage, a decoding stage (D), and address calculation stage (A) and an operation fetch stage (F). In contrast, Horvath et al. disclose a machine architecture for processing image blocks by the coordinated actions of an LSM and CODEC processors operating on image blocks stored in buffers. Thus, the machines would not work together, one being designed to process image blocks using primarily two processors and the other using several stages of a pipeline to process machine instructions.

Furthermore, the cited prior art does not disclose a "token" as recited in the claims of the present invention. A token of the present invention is defined in the specification as "interactive interfacing messenger package for control and /or data functions." This entails a technology more powerful than a traditional token, for example, in the context of token rings, or a traditional packet of information.

As to claim 2, Ueda discloses a bypass circuit allowing a memory fetch and write cycle to use the same data retrieved from memory without accessing the memory again. Ueda et al. does not disclose an "inactive state" (claim 2, line 2).

Therefore, the present invention recited in claims 1 and depending claims therefrom is not rendered obvious by the cited prior art.

VII. Rejection of claims under 35 U.S.C. § 103(a)

Claims 3-6 stand rejected under 35 U.S.C. § 103(a) as being

unpatentable over Horvath et al., in view of Ueda et al. and further in view of Schwartz. The Examiner concedes that Horvath and Ueda do not disclose the sequence of pipeline stages including at least one spatial decoder stage or one temporal decoder stage. The Examiner cites to Schwartz for this disclosure. However, Schwartz shows a microcomputer system for converting an analog signal into a digital form and storing it in a highly condensed code. To achieve this goal, Schwartz operates on streams of data, in contrast to Horvath et al. which operates on image blocks. Furthermore, Schwartz does not require the data to conform to any standard. Thus, the machines of Horvath et al and Schwartz being directed to different goals and operating on different data structures are not combinable. Additionally, Ueda, designed to process machine instructions is unrelated to Schwartz which is processing streams of audio or video data.

Therefore, the present invention recited in claims 3-6 is not rendered obvious by the cited prior art.

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VIII. Concluding Matters

In view of the foregoing remarks, it is respectfully submitted that each of the claims distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowance of all the pending claims is respectfully requested.

Should there be any remaining questions to correct format matters, it is urged that the Examiner contact the undersigned attorney with a telephone interview to expedite and complete prosecution.

If any further fees are required in connection with the filing of this response, please change same to our Deposit Account No. 04-1175.

Respectfully submitted,

DISCOVISION ASSOCIATES

Date: July 8, 2003

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